ABSTRACT OF THE DISCLOSURE

A ferroelectric memory of a 1T/1C type has a pair of dummy memory cells DMC2n-1 and DMC2n. Different information have been stored in the dummy memory cells. When the information is read out from each dummy memory cell, a potential Va is developed on a bit line BL2n-1, a potential Vb is developed on an adjacent bit line BL2n. Since the bit lines BL2n-1 and BL2n have the same capacitance, a potential Vave of each bit line which was short-circuited by a short-circuit portion s2a is equal to a just intermediate value (Va + Vb)/2 of the potentials Va and Vb. The potential Vave is applied to sense amplifiers SAn-1 and SAn as a reference potential.